CLAIMS

WHAT IS CLAIMED:

1. A device, comprising:

a circuit for performing an approximation of a current leakage associated with at least a portion of said device; and

a refresh rate control unit operatively coupled with said circuit, said refresh rate control unit comprising a refresh oscillator, said refresh rate control unit to adjust a refresh rate associated with at least a portion of said device in response to said approximation of said current leakage.

2. The device of claim 1, wherein said device is a memory device.

3. The device of claim 2, wherein said memory device is at least one of, a dynamic random access memory (DRAM), a double-data rate SDRAM (DDR SDRAM), a Rambus DRAM (RDRAM), and a FLASH memory.

4. The device of claim 1, wherein said circuit further comprises:

a first transistor to provide a first input signal;

a cell leakage model operatively coupled to said transistor, said cell leakage model to model a current leakage associated with at least a portion of said device;

a comparator to compare said first input signal to a reference input signal; and

a delay unit operatively coupled to said comparator, said delay unit to provide a delay upon an output from said comparator to provide a time period for pre-charging of said transistor and to provide a signal for controlling said refresh rate.

5. The device of claim 4, wherein said transistor is a P-channel transistor that is pulled up to a supply voltage.

6. The device of claim 4, wherein said transistor is an N-channel transistor that is pulled up to a supply voltage.

7. The device of claim 4, wherein said cell leakage model comprises a second transistor for modeling the current leakage of at least a portion of said device.

8. The device of claim 4, wherein said comparator comprises a differential amplifier.

9. The device of claim 4, wherein said comparator comprises a CMOS inverter.

10. The device of claim 4, wherein said delay unit comprises a plurality of inverters, wherein each of said plurality of inverters provides a delay.

11. The device of claim 1, wherein said leakage model circuit is capable of controlling said refresh rate associated with at least a portion of said device by adjusting the operation of said refresh oscillator.

12. The device of claim 1, wherein said circuit is capable of modeling a leakage current that is induced by a temperature level.

13. The device of claim 1, wherein said circuit is capable of modeling a leakage current that is induced by an operating voltage level.

14. The device of claim 1, wherein said circuit is capable of modeling a leakage current that is induced by a particular process feature associated with said device.

15. A circuit for controlling a refresh rate associated with at least a portion of a memory device, said circuit comprising:

a transistor to provide a first input signal;

a cell leakage model operatively coupled to said transistor, said cell leakage model to model a current leakage associated with at least a portion of said device;

a comparator to compare said first input signal to a reference input signal;

a delay unit operatively coupled to said comparator, said delay unit to provide a delay upon an output from said comparator to provide a time period for pre-charging of said transistor and to provide a signal for controlling said refresh rate; and

a refresh control oscillator operatively coupled to said delay unit, said refresh control oscillator to provide said refresh rate for refreshing at least said portion of said memory device.

16. The circuit of claim 15, wherein said cell leakage model is capable of modeling a leakage current that is induced by a temperature level.

17. The circuit of claim 15, wherein said cell leakage model is capable of modeling a leakage current that is induced by an operating voltage level.

18. The circuit of claim 15, wherein said cell leakage model is capable of modeling a leakage current that is induced by a particular process feature associated with said device.

19. A system board, comprising:

a processor;

a memory device operatively coupled to said processor, said memory device comprising:

a leakage model circuit for performing an approximation of a current leakage associated with a portion of said device; and

a refresh rate control unit operatively coupled with said leakage model circuit, said refresh rate control unit comprising a refresh oscillator, said refresh rate control unit to adjust a refresh rate associated with at least a portion of said memory device in response to said approximation of said current leakage.

20. The system board described in claim 19, wherein said memory device is at least one of a DRAM, a DDR SDRAM, a RDRAM, and a FLASH memory.

21. The system board of claim 19, wherein said system board is a motherboard of a computer system.

22. The system board of claim 19, wherein said leakage model circuit further comprises:

a transistor to provide a first input signal;

a cell leakage model operatively coupled to said transistor, said cell leakage model to model said current leakage associated with at least a portion of said device;

a comparator to compare said first input signal to a reference input signal; and

a delay unit operatively coupled to said comparator, said delay unit to provide a delay upon an output from said comparator to provide a time period for pre-charging of said transistor and to provide a signal for controlling said refresh rate.

23. The system board of claim 22, wherein said transistor is a P-channel transistor that is pulled up to a supply voltage.

24. The system board of claim 22, wherein said comparator comprises a differential amplifier.

25. The system board of claim 22, wherein said delay unit comprises a plurality of inverters, wherein each of said plurality of inverters provides a delay.

26. The system board of claim 19, wherein said leakage model circuit is capable of controlling said refresh rate associated with at least a portion of said device by adjusting the operation of said refresh oscillator.

27. The system board of claim 19, wherein said leakage model circuit is capable of modeling said leakage current that is induced by a temperature level.

28. The system board of claim 19, wherein said leakage model circuit is capable of modeling a leakage current that is induced by an operating voltage level.

29. The system board of claim 19, wherein said leakage model circuit is capable of modeling a leakage current that is induced by a particular process feature associated with said device.

30. A memory device, comprising:

a leakage model circuit for performing an approximation of a current leakage associated with a portion of said device; and

a refresh rate control unit operatively coupled with said leakage model circuit, said refresh rate control unit comprising a refresh oscillator, said refresh rate control unit to adjust a refresh rate associated with at least a portion of said device in response to said approximation of said current leakage.

31. The memory device of claim 30, wherein said memory device is at least one of a dynamic random access memory (DRAM), a double-data rate SDRAM (DDR SDRAM), a Rambus DRAM (RDRAM), and a FLASH memory.

32. The memory device of claim 30, wherein said leakage model circuit further comprises:

a transistor to provide a first input signal;

a cell leakage model operatively coupled to said transistor, said cell leakage model to model said current leakage associated with at least a portion of said device;

a comparator to compare said first input signal to a reference input signal; and

a delay unit operatively coupled to said comparator, said delay unit to provide a delay upon an output from said comparator to provide a time period for pre-charging of said transistor and to provide a signal for controlling said refresh rate.

33. The memory device of claim 32, wherein said transistor is a P-channel transistor that is pulled up to a supply voltage.

34. The memory device of claim 32, wherein said comparator comprises a differential amplifier.

35. The memory device of claim 32, wherein said delay unit comprises a plurality of inverters, wherein each of said plurality of inverters provides a delay.

36. The memory device of claim 30, wherein said leakage model circuit is capable of controlling said refresh rate associated with at least a portion of said device by adjusting the operation of said refresh oscillator.

37. The memory device of claim 30, wherein said leakage model circuit is capable of modeling a leakage current that is induced by a temperature level.

38. The memory device of claim 30, wherein said leakage model circuit is capable of modeling a leakage current that is induced by an operating voltage level.

39. The memory device of claim 30, wherein said leakage model circuit is capable of modeling a leakage current that is induced by a particular process feature associated with said device.

40. A method, comprising:

detecting a change in a current leakage relating to at least a portion of a memory device; and

adjusting a refresh rate associated with said portion of said memory device in response to detecting said current leakage.

41. The method of claim 40, wherein detecting a change in said current leakage further comprises modeling said current leakage relating at least a portion of said memory device.

42. The method of claim 41, wherein modeling said current leakage further comprises detecting a change in said current leakage in response to a change in a temperature level.

43. The method of claim 41, wherein modeling said current leakage further comprises detecting a change in said current leakage in response to a change in an operating voltage level.

44. The method of claim 40, wherein adjusting a refresh rate associated with said portion of said memory device further comprises modifying the operation of a refresh oscillator.

45. An apparatus, comprising:

means for detecting a change in a current leakage relating to at least a portion of a memory device; and

means for adjusting a refresh rate associated with said portion of said memory device in response to detecting said current leakage.

46. A computer readable program storage device encoded with instructions that, when executed by a computer, performs a method, comprising:

detecting a change in a current leakage relating to at least a portion of a memory device; and

adjusting a refresh rate associated with said portion of said memory device in response to detecting said current leakage.

47. The computer readable program storage device encoded with instructions that, when executed by a computer, performs the method of claim 46, wherein detecting a change in said current leakage further comprises modeling said current leakage relating at least a portion of said memory device.

48. The computer readable program storage device encoded with instructions that, when executed by a computer, performs the method of claim 47, wherein modeling said current leakage further comprises detecting a change in said current leakage in response to a change in a temperature level.

49. The computer readable program storage device encoded with instructions that, when executed by a computer, performs the method of claim 47, wherein modeling said current leakage further comprises detecting a change in said current leakage in response to a change in an operating voltage level.

50. The computer readable program storage device encoded with instructions that, when executed by a computer, performs the method of claim 46, wherein adjusting said refresh rate associated with said portion of said memory device further comprises modifying the operation of a refresh oscillator.

51. A computer system, comprising:

a display device;

a computer unit operatively coupled to said display device, said computer unit comprising a system board, said system board comprising:

a processor;

a memory device operatively coupled to said processor, said memory device comprising:

a leakage model circuit for performing an approximation of a current leakage associated with a portion of said device; and

a refresh rate control unit operatively coupled with said leakage model circuit, said refresh rate control unit comprising a refresh oscillator, said refresh rate control unit to adjust a refresh rate associated with at least a portion of said

memory device in response to said approximation of said current leakage.

52. The computer system described in claim 51, wherein said display device is a monitor.

53. The computer system described in claim 51, wherein said memory device is at least one of a DRAM, a DDR SDRAM, a RDRAM, and a FLASH memory.

54. The computer system of claim 51, wherein said system board is a motherboard of a computer system.

55. The computer system of claim 51, wherein said leakage model circuit further comprises:

a transistor to provide a first input signal;

a cell leakage model operatively coupled to said transistor, said cell leakage model to model said current leakage associated with at least a portion of said device;

a comparator to compare said first input signal to a reference input signal; and

a delay unit operatively coupled to said comparator, said delay unit to provide a delay upon an output from said comparator to provide a time period for pre-charging of said transistor and to provide a signal for controlling said refresh rate.

56. The computer system of claim 51, wherein said portion of said memory device comprises at least one memory cell.